REMARKS

The Office Action dated December 18, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claim 3 has been amended, and claims 1-2 have been cancelled without prejudice. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 3-12 are pending in the present application and are respectfully submitted for consideration.

Claims 1-3 were rejected under 35 U.S.C. § 102(b) as being anticipated by Marbot (U.S. Patent No. 5,268,937, "Marbot"). Claims 1 and 2 have been canceled, and claim 3 has been amended to depend on independent claim 4. In view of these amendments, Applicants submit that the rejection is now moot.

Claims 1-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yarborough, Jr. (U.S. Patent No. 4,454,499, "Yarborough") and further in view of Chieco et al. (U.S. Patent No. 5,912,928, "Chieco"). Applicants respectfully submit that each of claims 3-12 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 4 recites a method of transferring an encoded data signal including a clock signal and a data signal. The method comprising the steps of decoding the encoded data signal to generate a decoded data signal and a write clock signal, storing the decoded data signal in a memory in accordance with the write clock signal, determining

a transfer speed of the encoded data signal using the write clock signal, and generating a read clock signal having a frequency corresponding to the determined data transfer speed. In addition, the method comprising the steps of reading the decoded data signal stored in the memory in accordance with the read clock signal, and encoding the read decoded data signal and the read clock signal to generate an encoded data signal.

Claim 9 recites an apparatus for transferring an encoded data signal including a clock signal and a data signal. The apparatus includes a decoder circuit for decoding the encoded data signal to generate a decoded data signal and write clock signal, a memory, connected to the decoder circuit, for storing the decoded data signal in accordance with the write clock signal, a transfer speed determining circuit for determining a transfer speed of the encoded data signal in accordance with the write clock signal, wherein the transfer speed determining circuit generates a read clock signal having a frequency corresponding to the determined transfer speed, and the decoded data signal is read from the memory in accordance with the read clock signal, and an encoder circuit, connected to the memory and the transfer speed determining circuit, for encoding the decoded data signal and the read clock signal to generate the encoded data signal.

Accordingly, at least the essential features of the present invention is the steps of "decoding the encoded data signal to generate a decoded data signal and a write clock signal," and "storing the decoded data signal in a memory in accordance with the write clock signal" with respect to claim 4, and at least the essential features of "an decoder circuit for decoding the encoded data signal to generate a decoded data signal and

write clock signal" and "a memory, connected to the decoder circuit, for storing the decoded data signal in accordance with the write clock signal" with respect to claim 9. As such, the present invention results in the advantage of determining a data transfer speed that has an improved data transfer speed.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 3-12, and therefore fails to provide the advantages that are provided by the present application.

Yarborough, Jr. discloses a digital decoder for Miller encoded signals having a resettable counter which is clocked at a frequency which is a large multiple of the base frequency of the Miller encoded signal. Transitions in the Miller encoded data stream are used to reset the counter. Yarborough, Jr. shows a digital signal storage means for storing a digital signal having a value substantially equal to the value to which the counter is advanced in one Miller unit of time, and an output logic circuit means responsive to outputs from the counter and digital signal storage means for producing a binary output signal indicative of the decoded Miller encoded input signal. In addition, Yarborough discloses means for recurrently updating the contents of the digital signal storage means to adjust for variations in the base frequency of the Miller encoded input signal.

Chieco discloses a clock encoding circuit for high speed data transmission, e.g., for Manchester encoding, and a circuit for controlling transmitting data and the encoded clock. The clock encoding circuit of Chieco includes two parallel to serial shift registers receiving parallel DATA and shifting at the data transmission rate. One of the registers

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receives every other bit of the data inverted. When both registers are clocked at the data transmission rate, DATA is shifted out of the register with uninverted bits, and the transmission clock is encoded in STROBE, which is shifted out of the serial output of the other register. Bit inversion may be with invertors receiving data as it is passed in parallel to both registers, or alternatively, after it is loaded into the one (DATA) register.

Applicants respectfully submit that each and every element recited within claims 4 and 9 is neither disclosed nor suggested by Yarborough, Jr. and Chieco, taken alone or in combination. In particular, Applicants submit that the method and an apparatus of transferring an encoded data signal, wherein the encoded data signal includes a clock signal and a data signal as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limiting elements of "decoding the encoded data signal to generate a decoded data signal and a write clock signal," and "storing the decoded data signal in a memory in accordance with the write clock signal" with respect to claim 4, and at least the essential features of "an decoder circuit for decoding the encoded data signal to generate a decoded data signal and write clock signal" and "a memory, connected to the decoder circuit, for storing the decoded data signal in accordance with the write clock signal" with respect to claim 9.

Applicants submit that Yarborough fails to disclose the decoder circuit for and the step of generating a write clock signal by decoding an encoded data signal to store the decoded data signal in a memory in accordance with the write clock signal. Yarborough merely discloses an encoded data signal (Miller input), but the Miller input does not

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include a clock signal. As shown in Fig. 2 of Yarborough, the Miller input does not periodically generate an edge, which means that the Miller input does not include a periodic clock signal. Therefore, Yarborough internally generates a write clock signal and writes data in the flip-flop 30 in accordance with the internally generated write clock signal.

In contrast, the present invention provides an encoded data signal <u>includes both a clock signal and a data signal</u>. Since the encoded data signal of the present invention includes both a clock signal and a data signal, a write clock signal can be generated by decoding the encoded data signal without the need for internal process for obtaining a write clock signal.

In addition, Chieco merely discloses generating a clock signal using a strobe signal and a data signal by an IC chip 110. However, Chieco does not disclose generating a write clock signal by decoding an encoded data signal to store the decoded data signal in a memory in accordance with the write clock signal.

Accordingly, Applicants submit that neither Yarborough nor Chieco, taken singularly or in combination, disclose or suggest each and every element recited in claims 4 and 9 of the present application, and therefore is allowable.

As claims 3, 5-8 depend from claim 4, and claims 10-12 depends from claim 9, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims.

In view of the above, Applicants respectfully submit that each of claims 3-12 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 3-12 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108075-00033.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (2 months)